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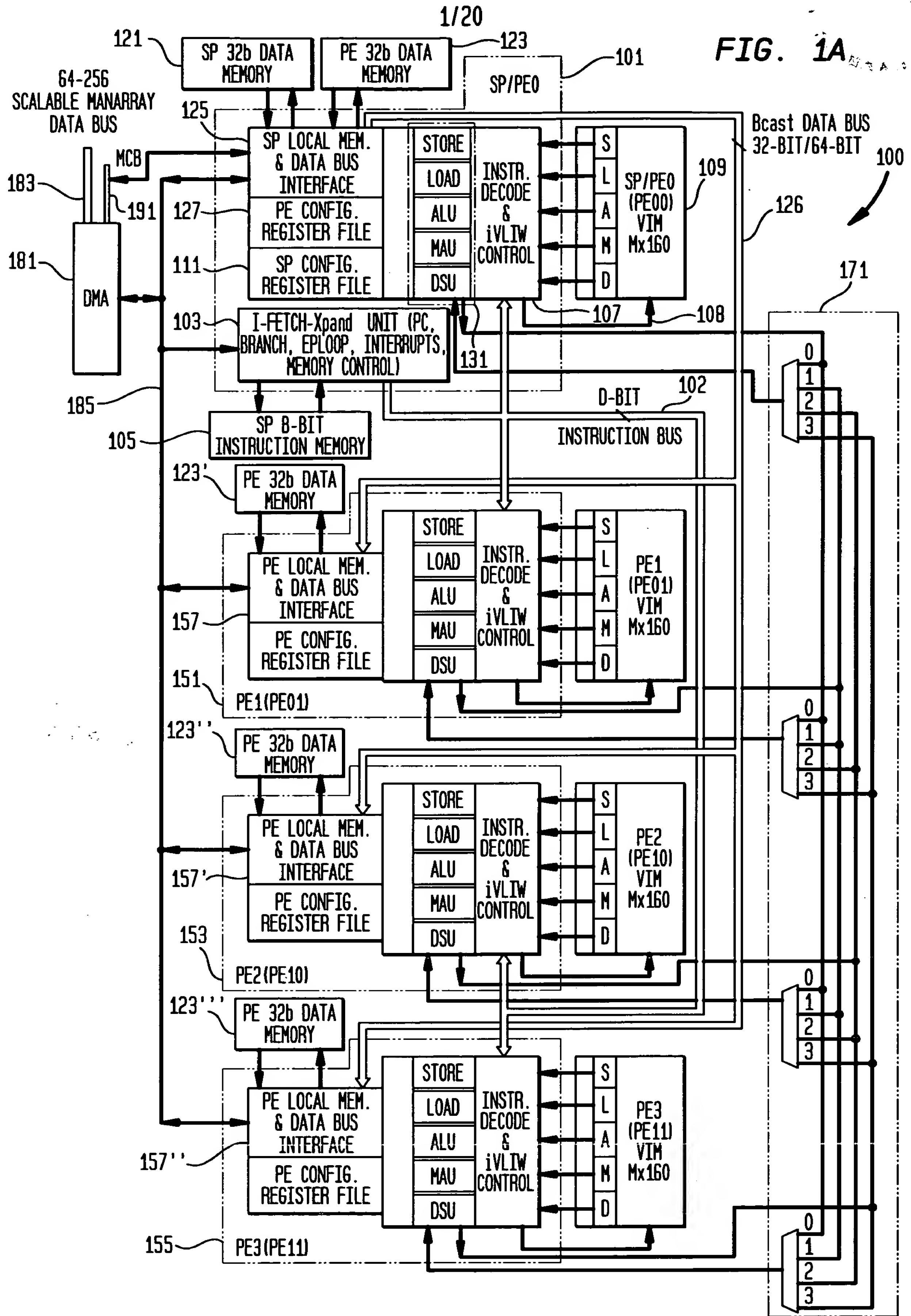
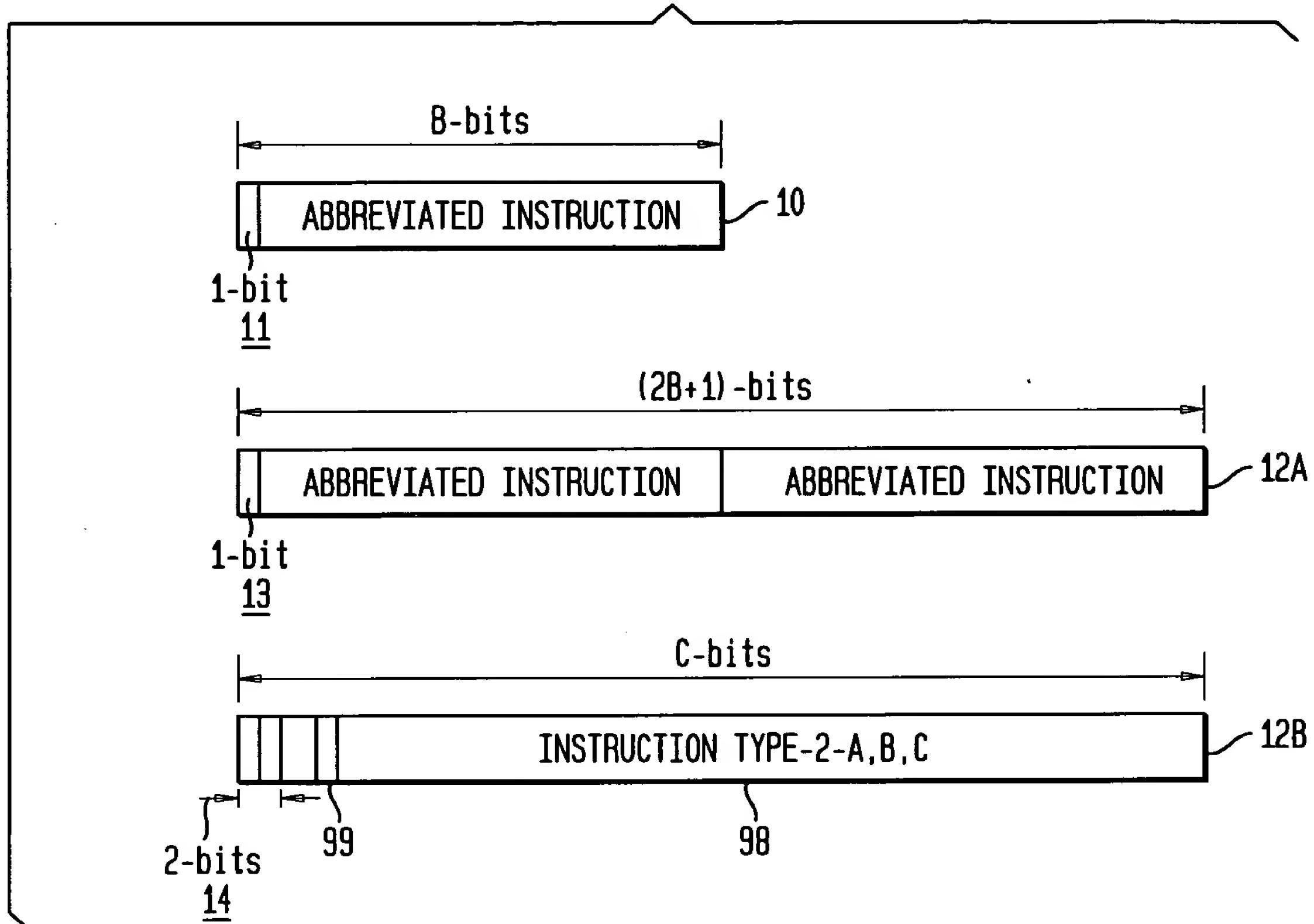
SERIAL NO.: 09/422,015
PETER H. PRIEST (919-942-1434)

FIG. 1A

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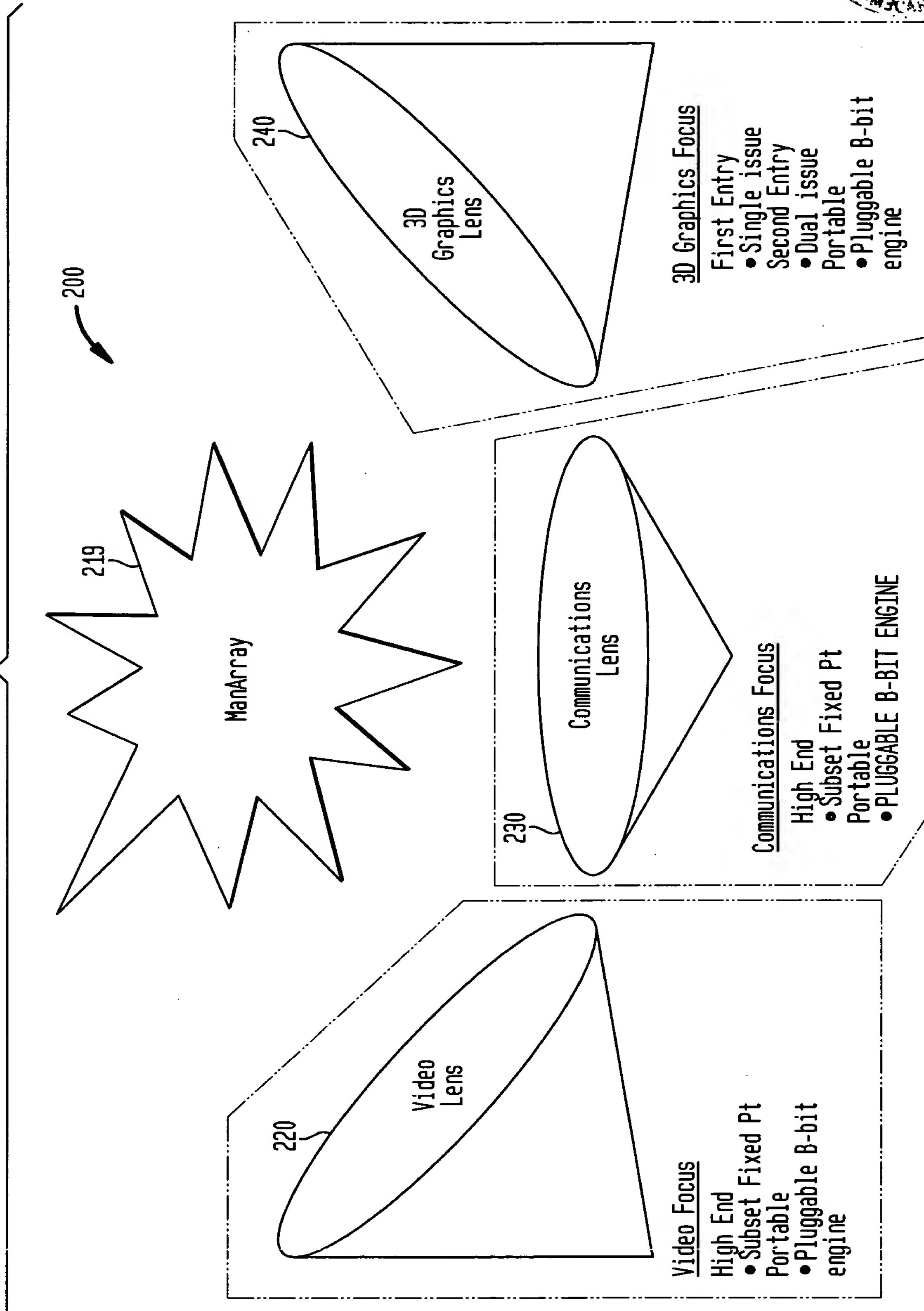
FIG. 1B



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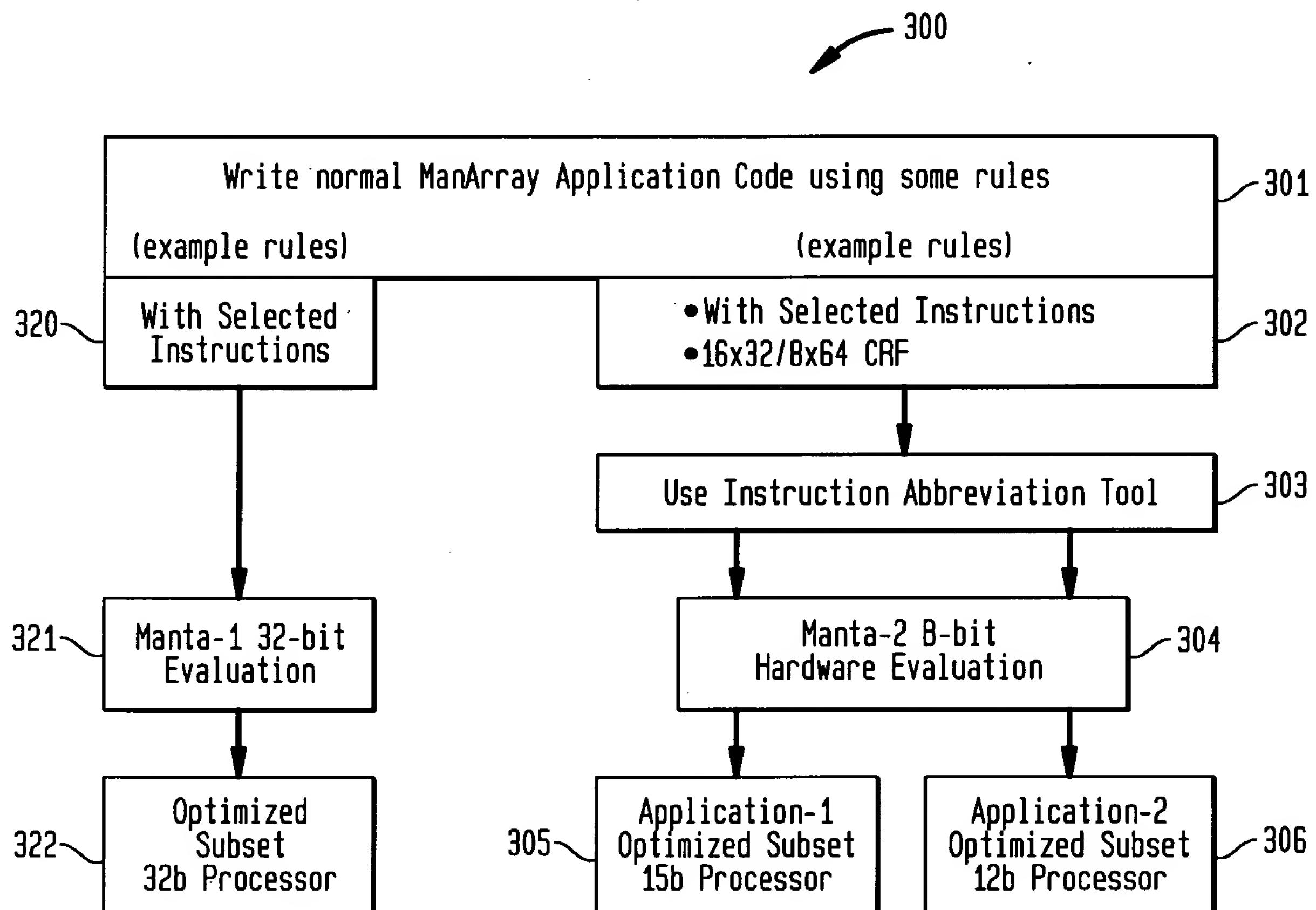
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FIG. 2



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FIG. 3A



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FIG. 3B

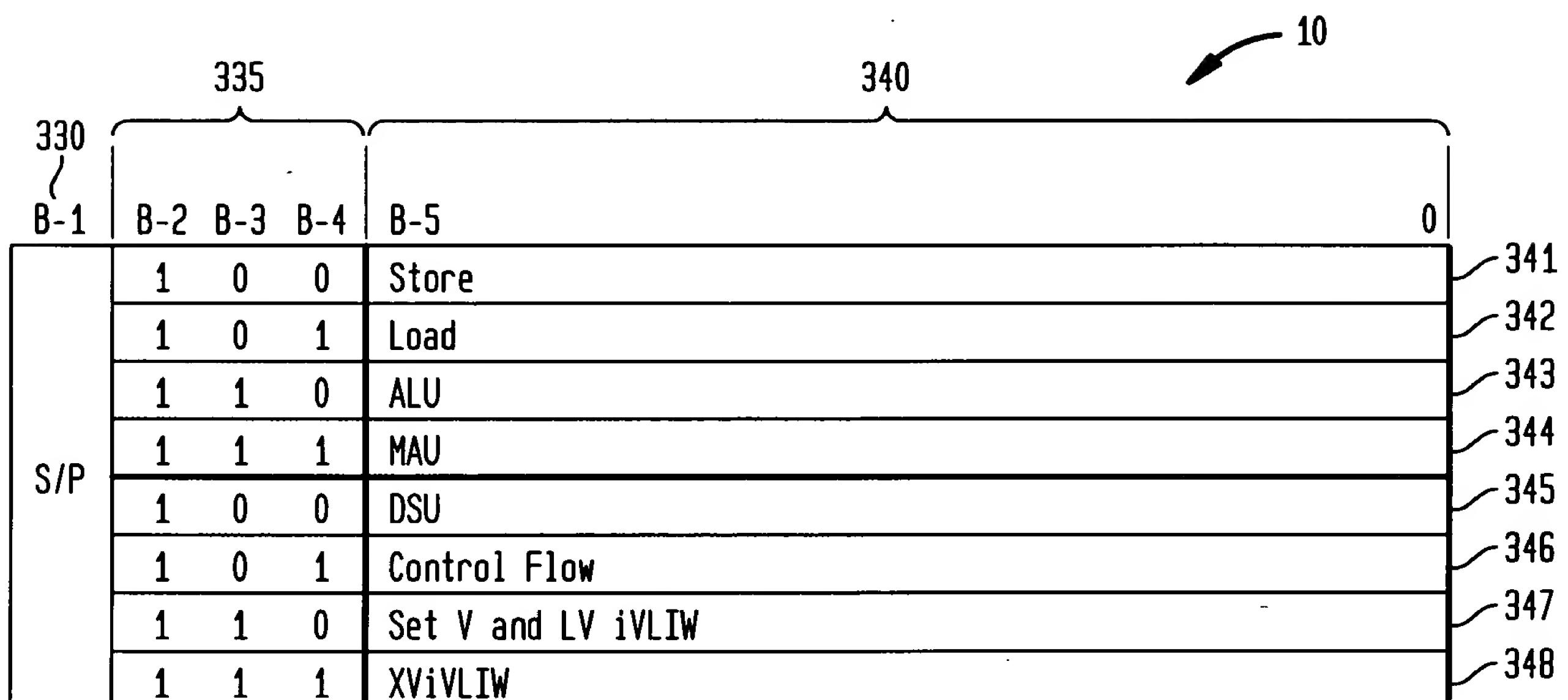
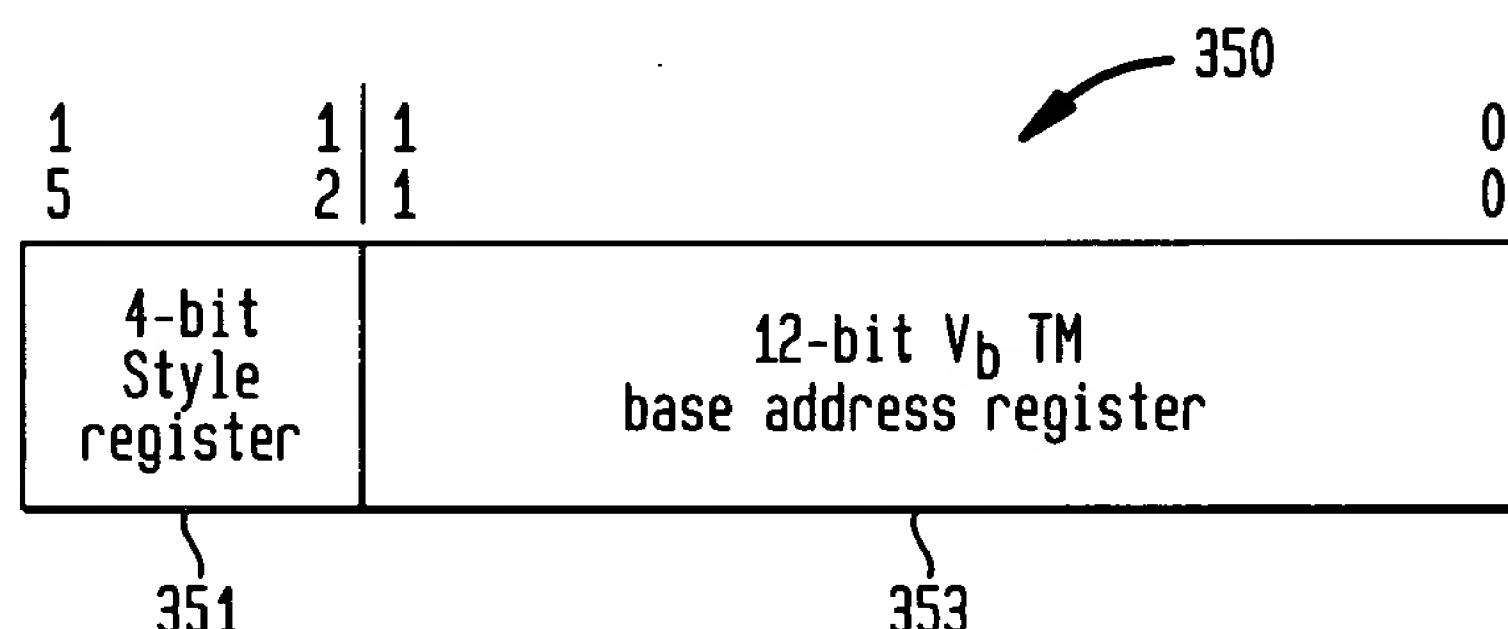


FIG. 3C



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FIG. 3D

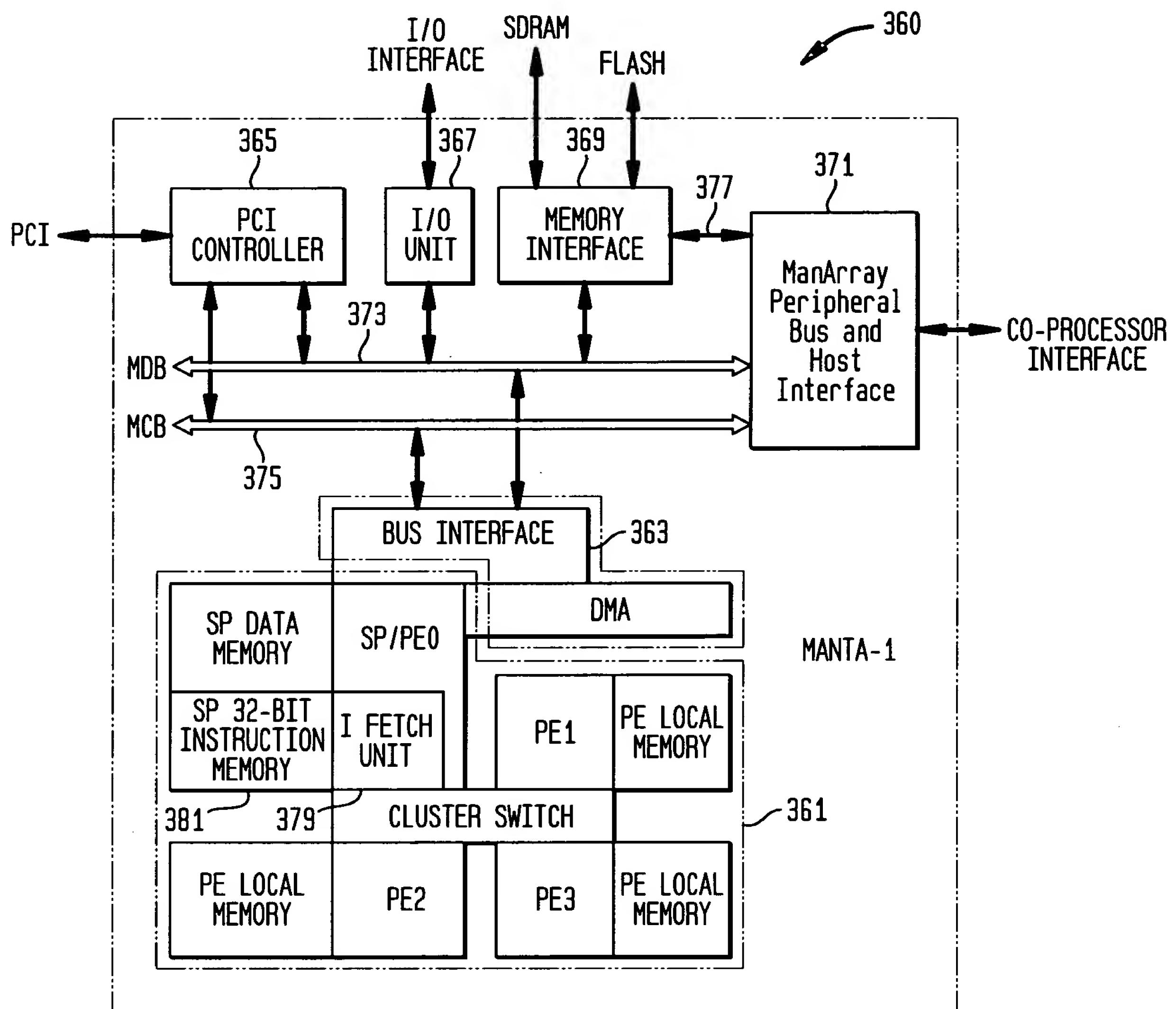
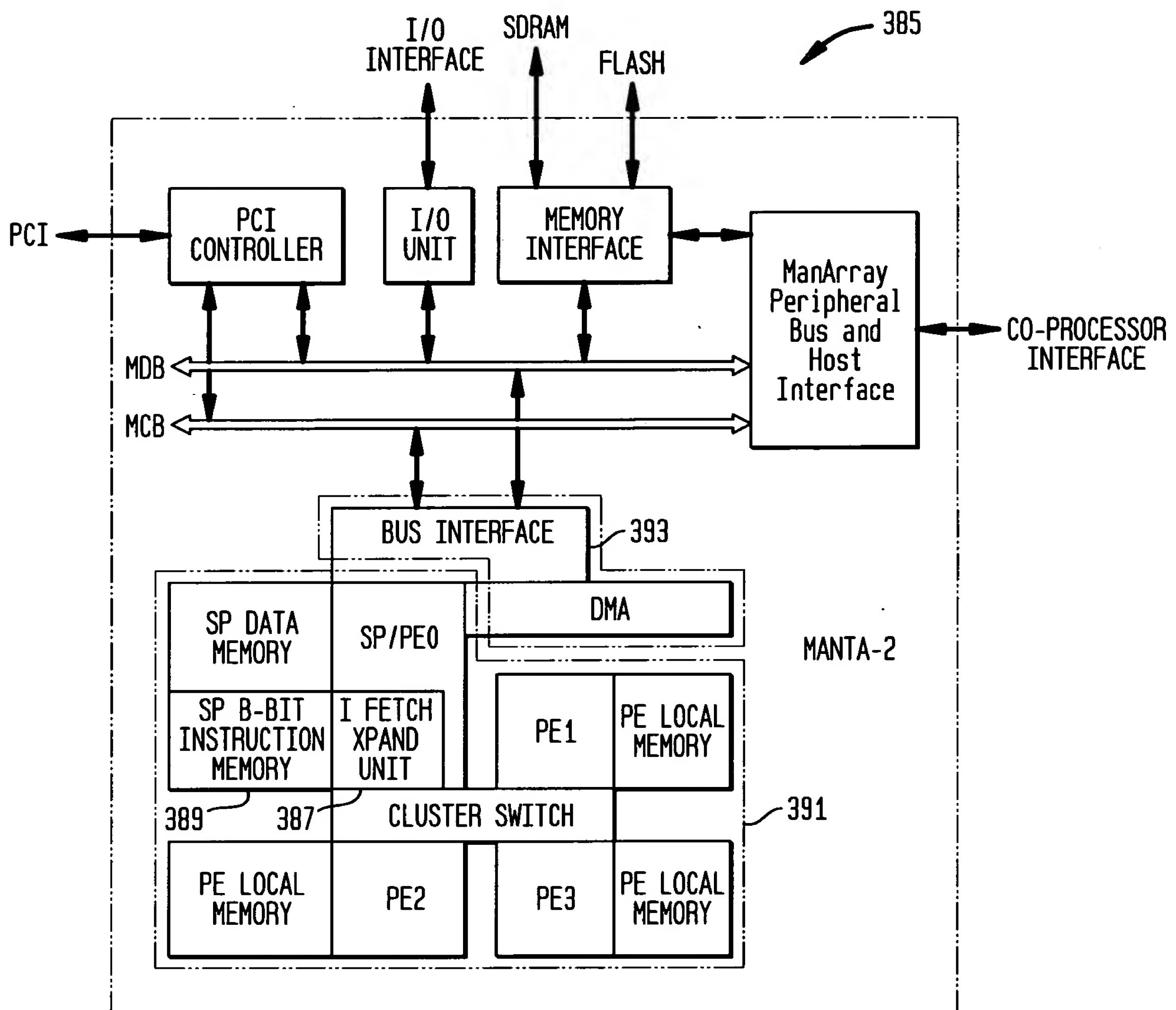
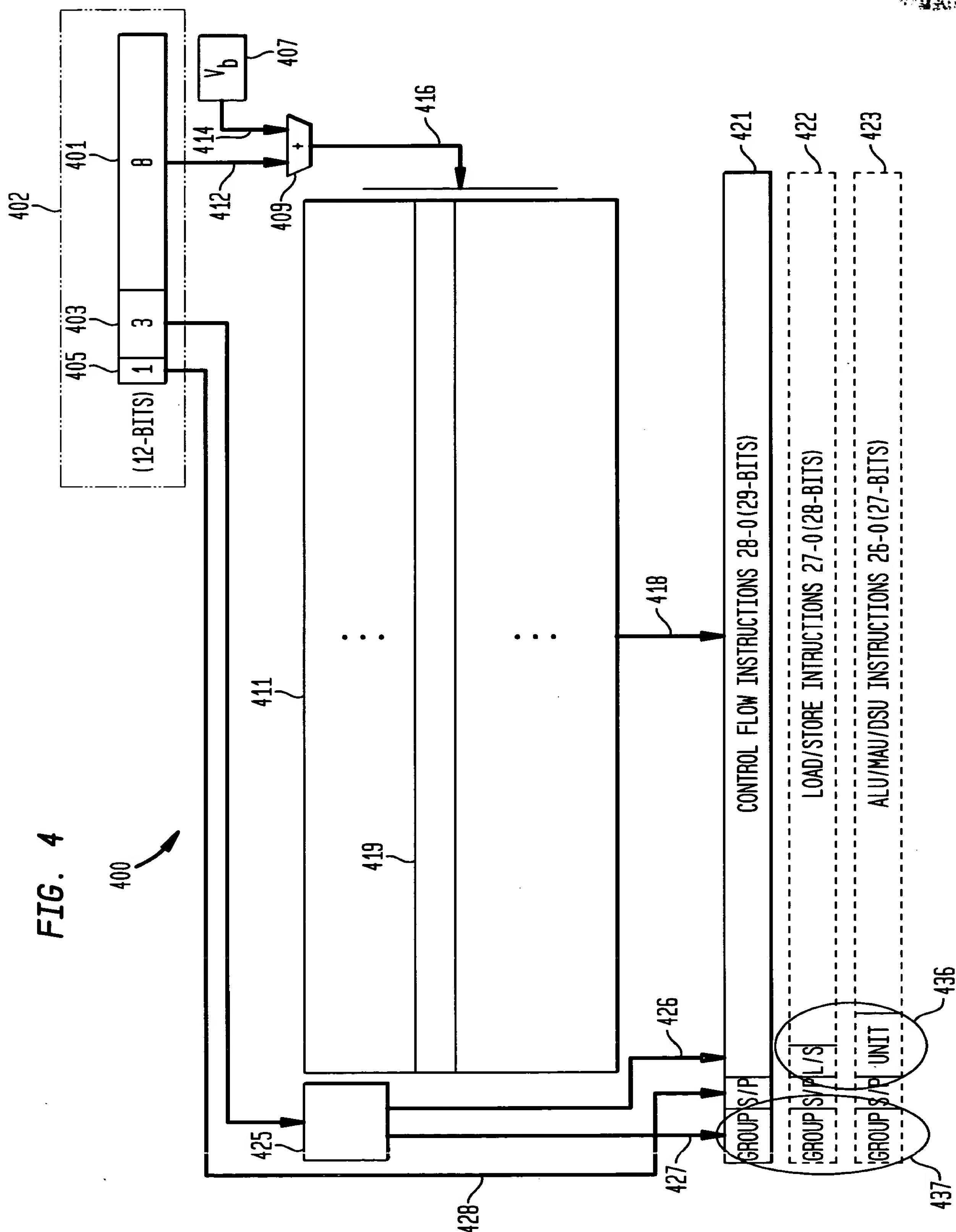


FIG. 3E



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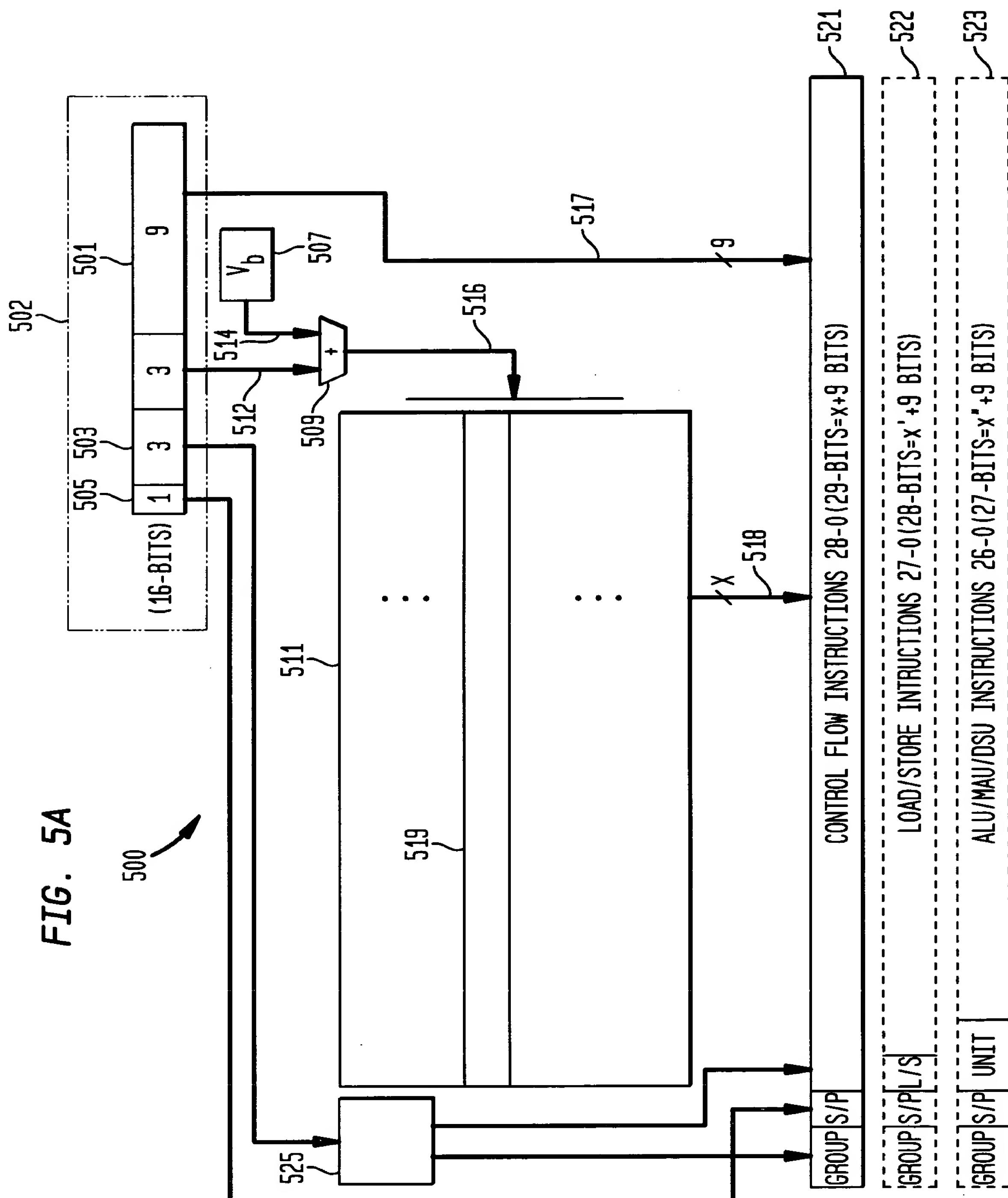
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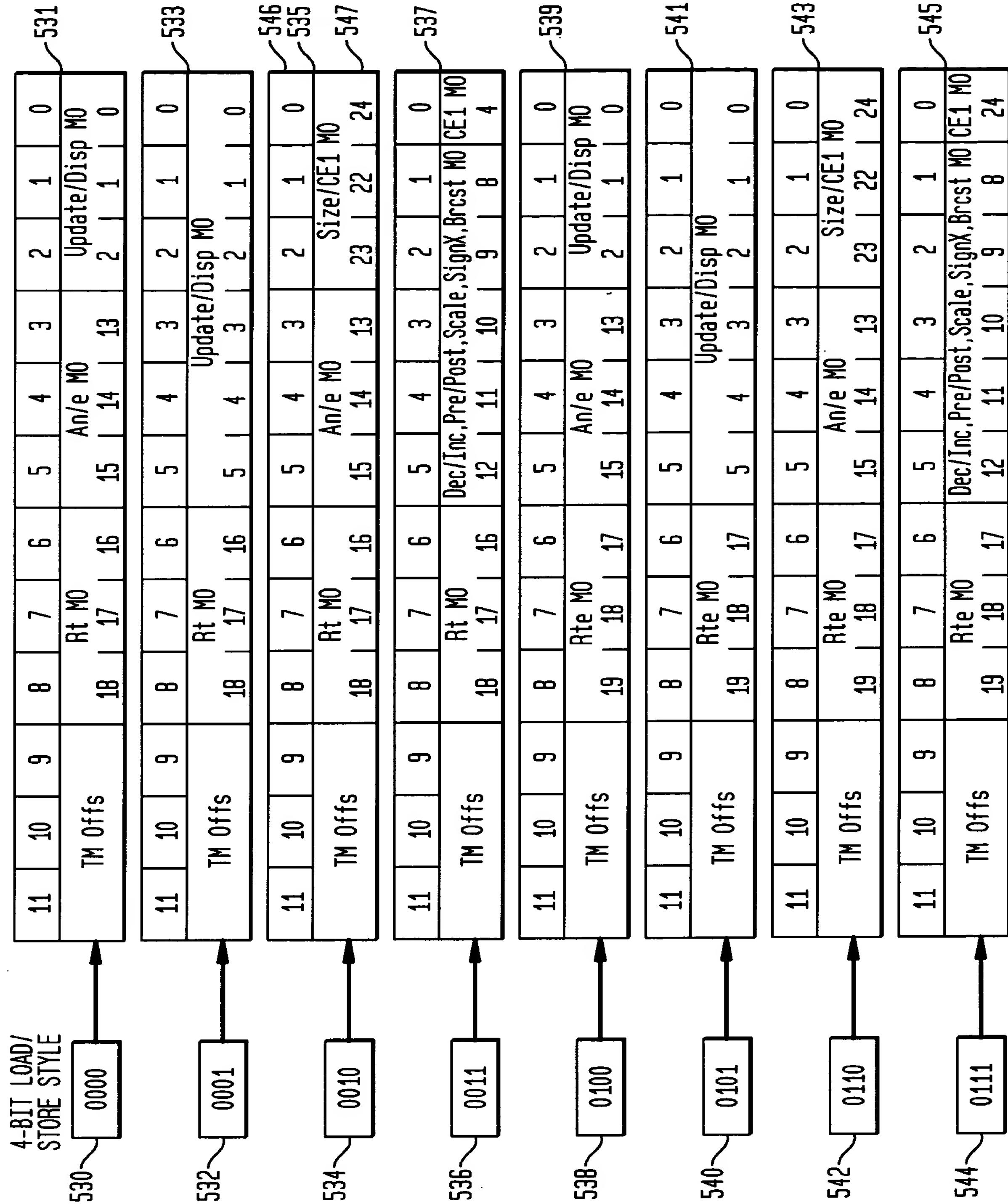
FIG. 5A



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FIG. 5B



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FIG. 5C

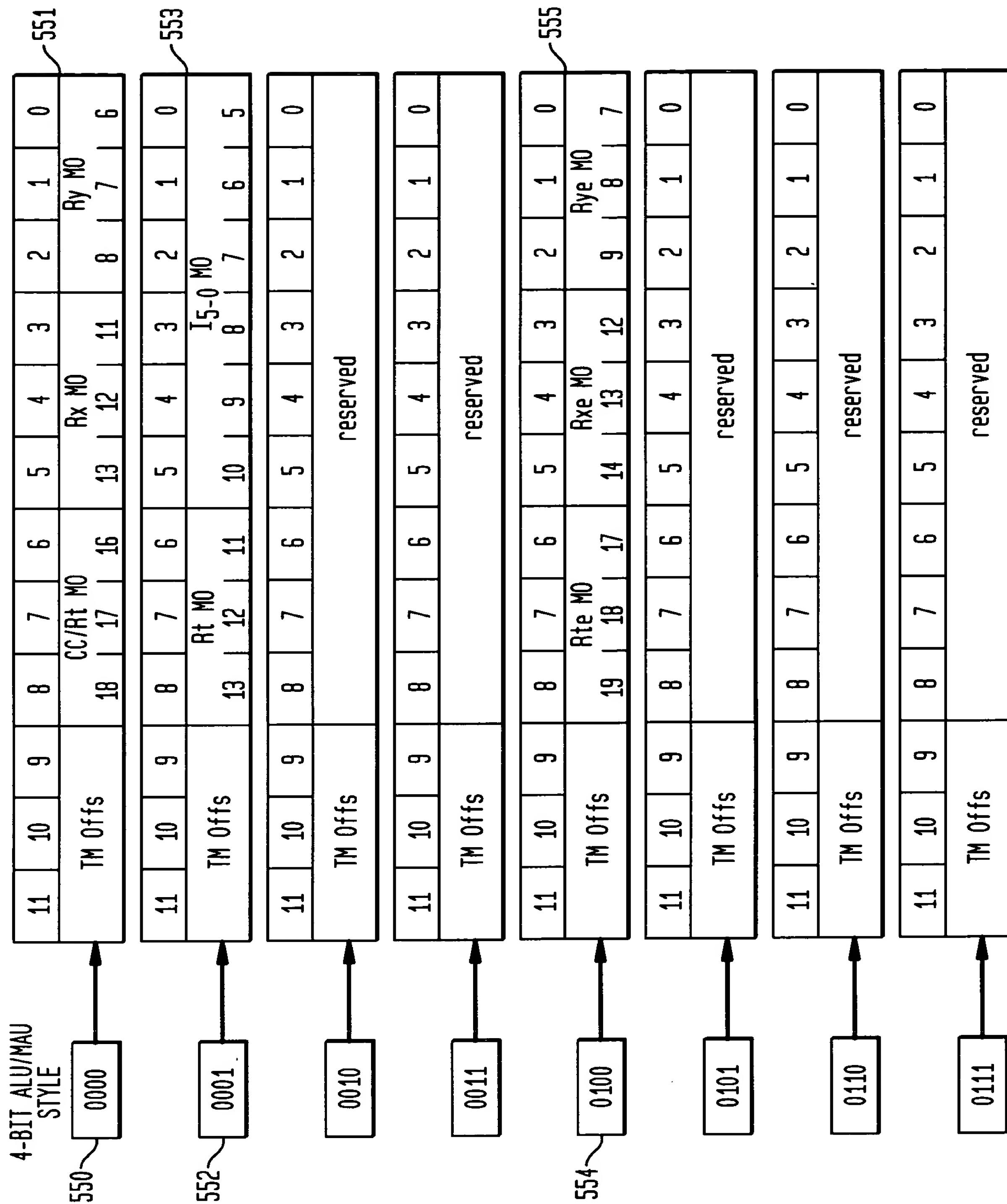
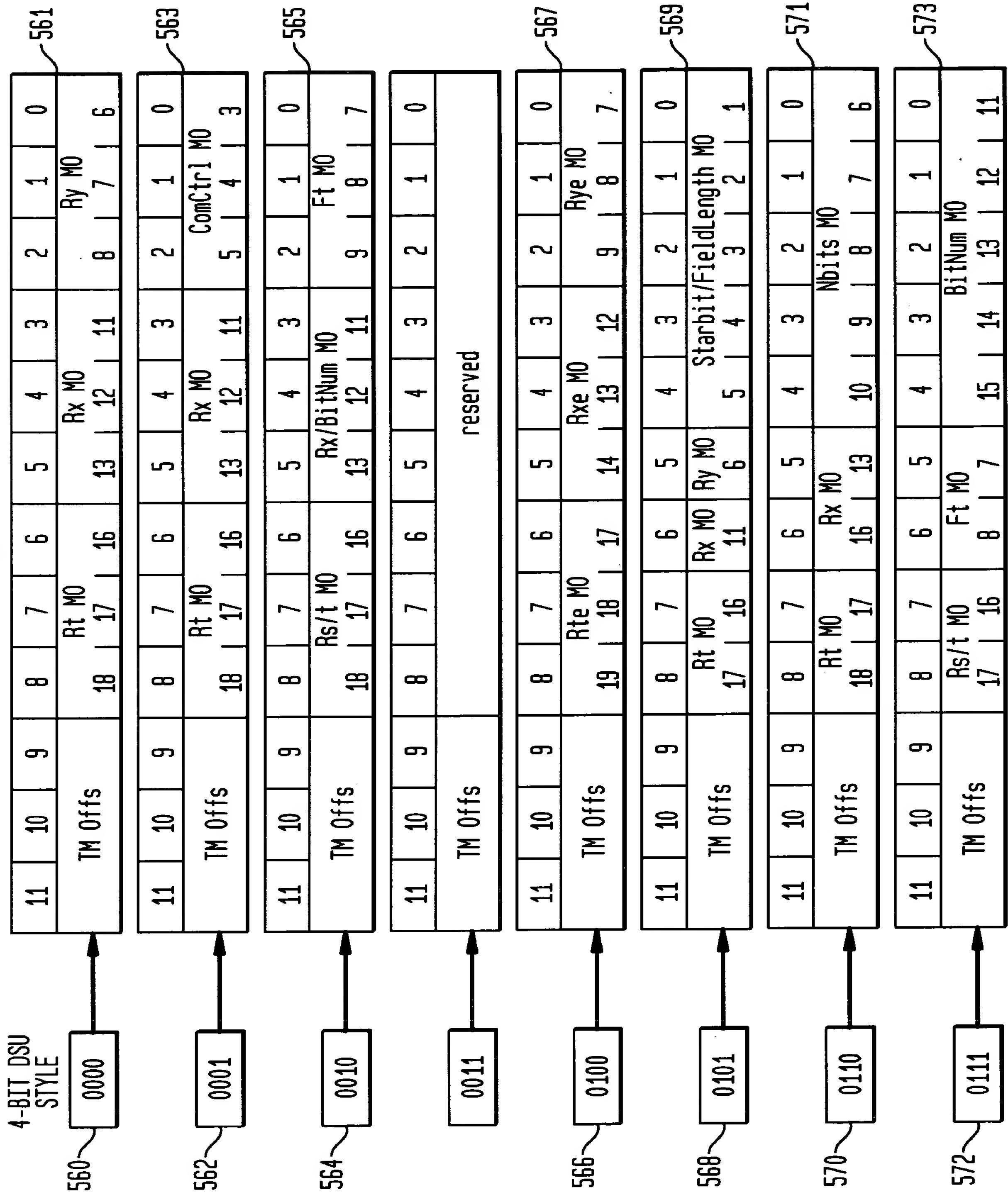


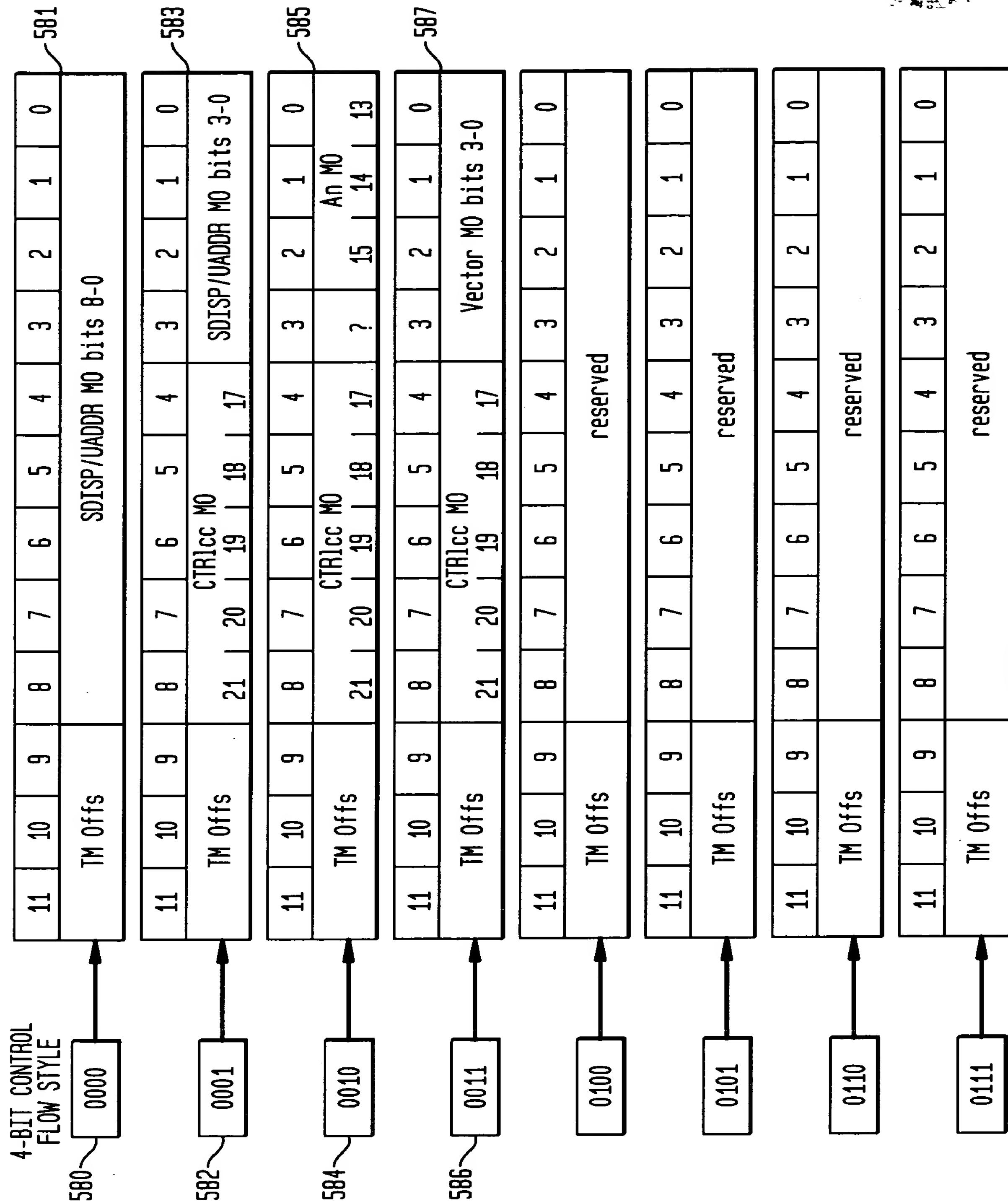
FIG. 5D



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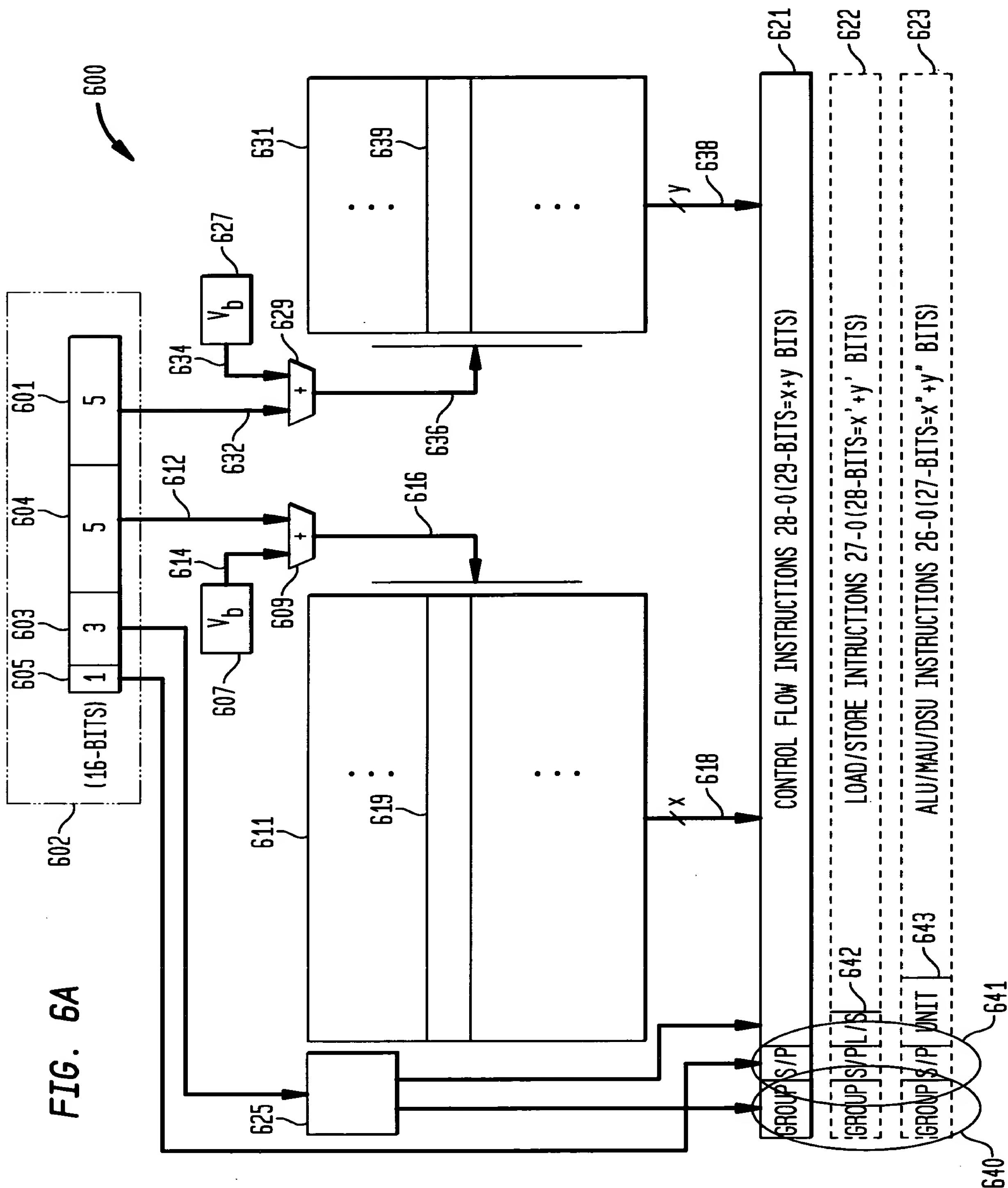
FIG. 5E



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FIG. 6A

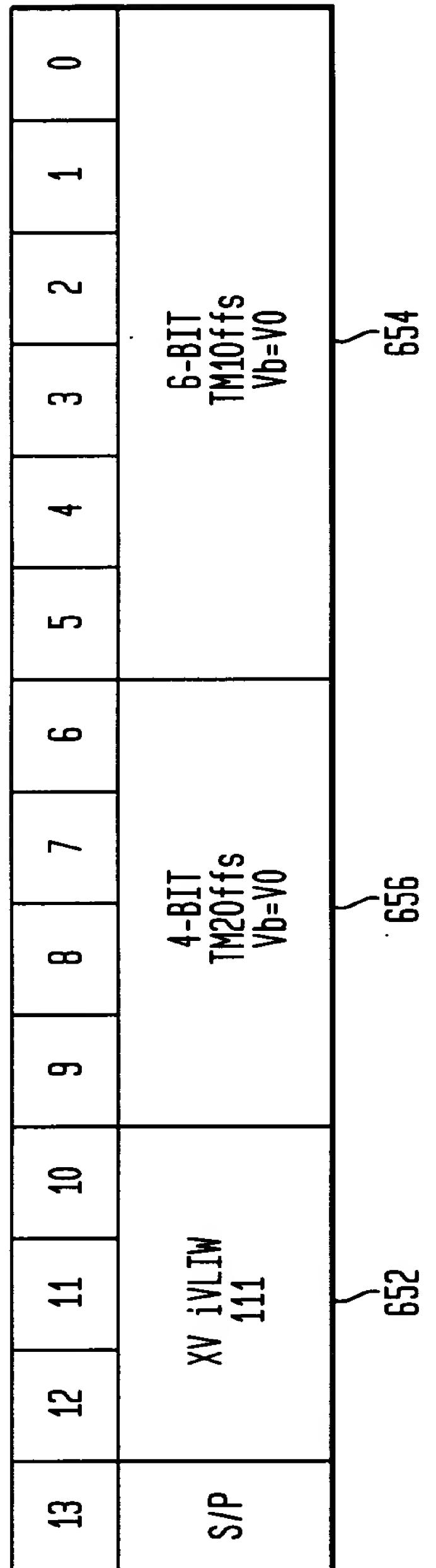


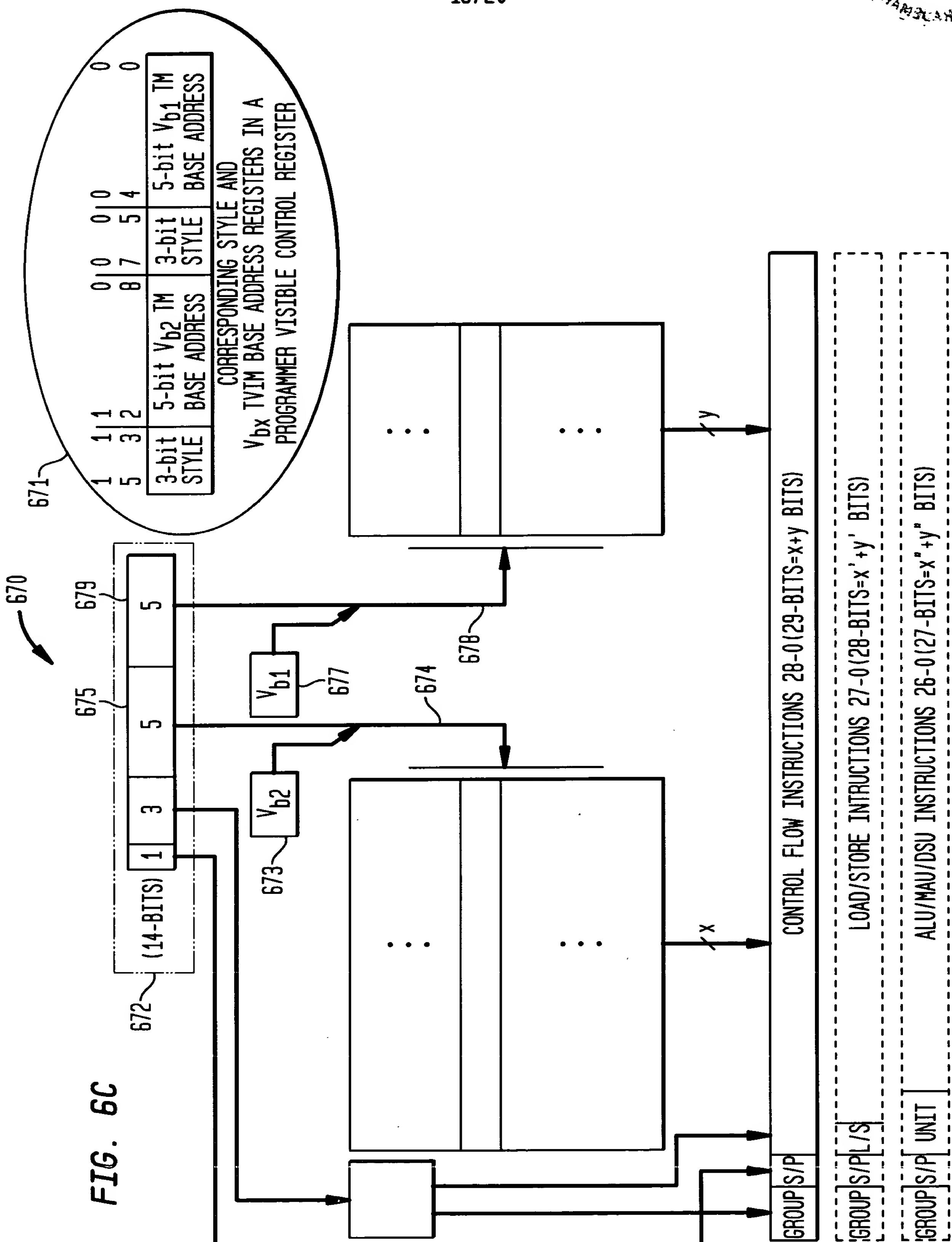
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FIG. 6B

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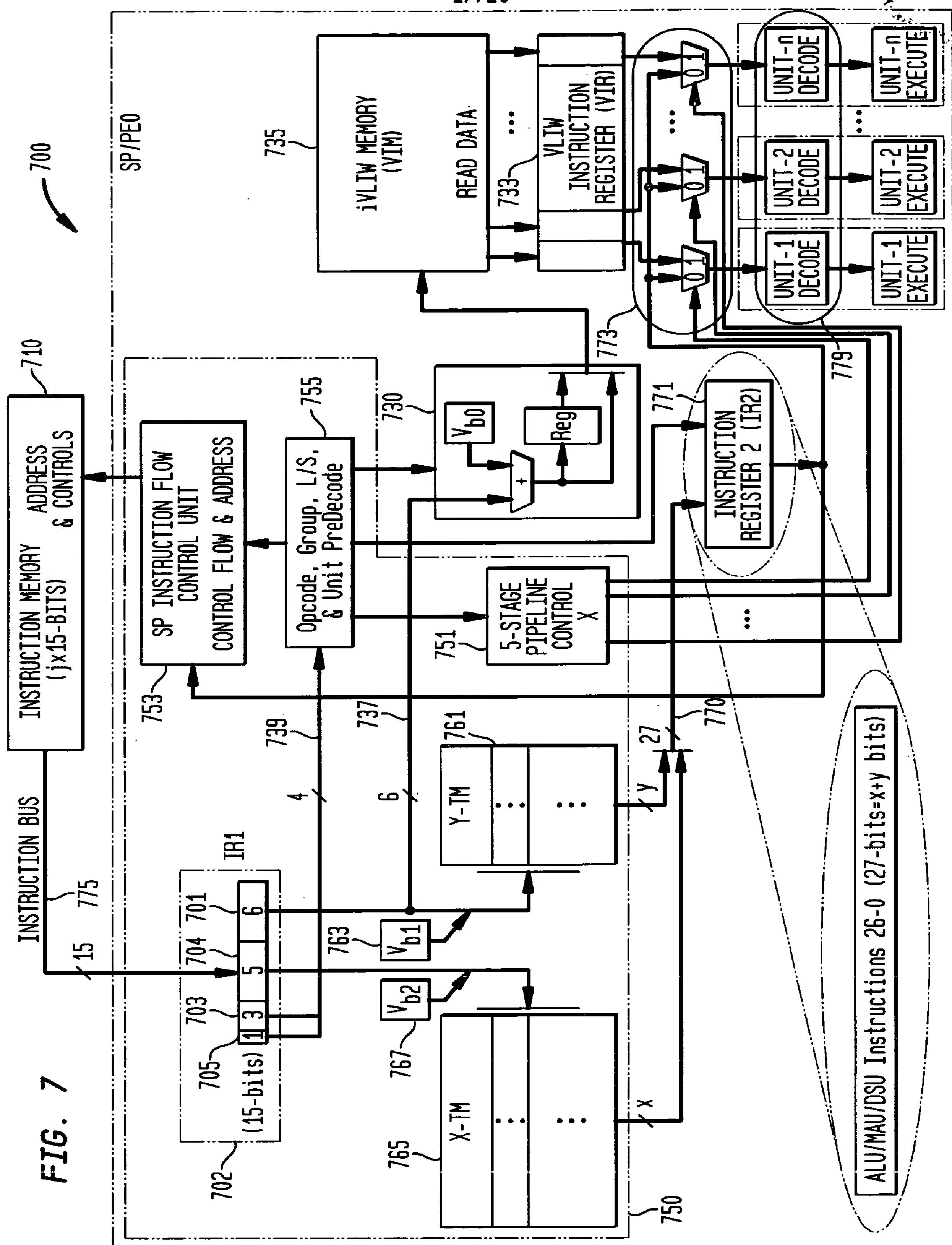
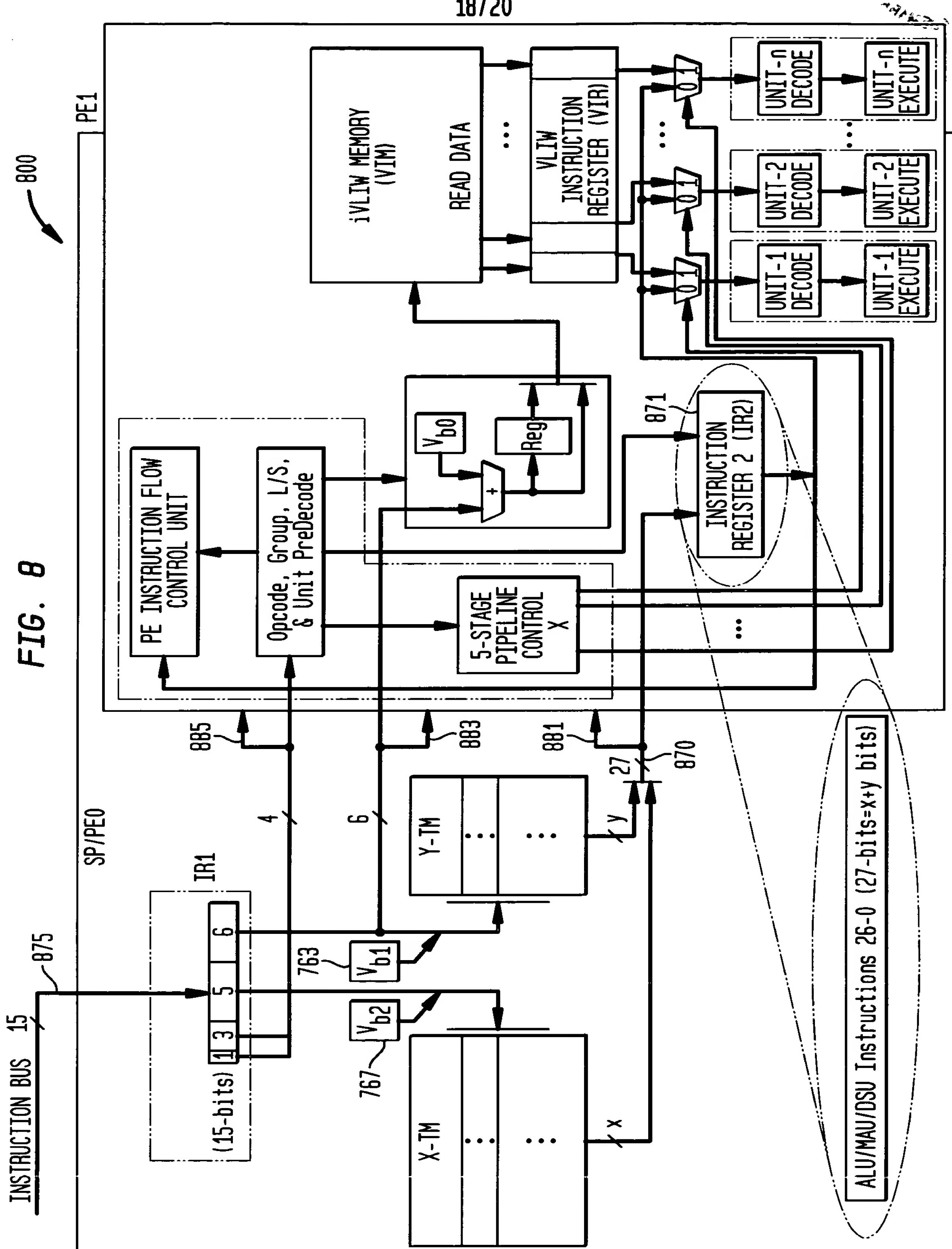


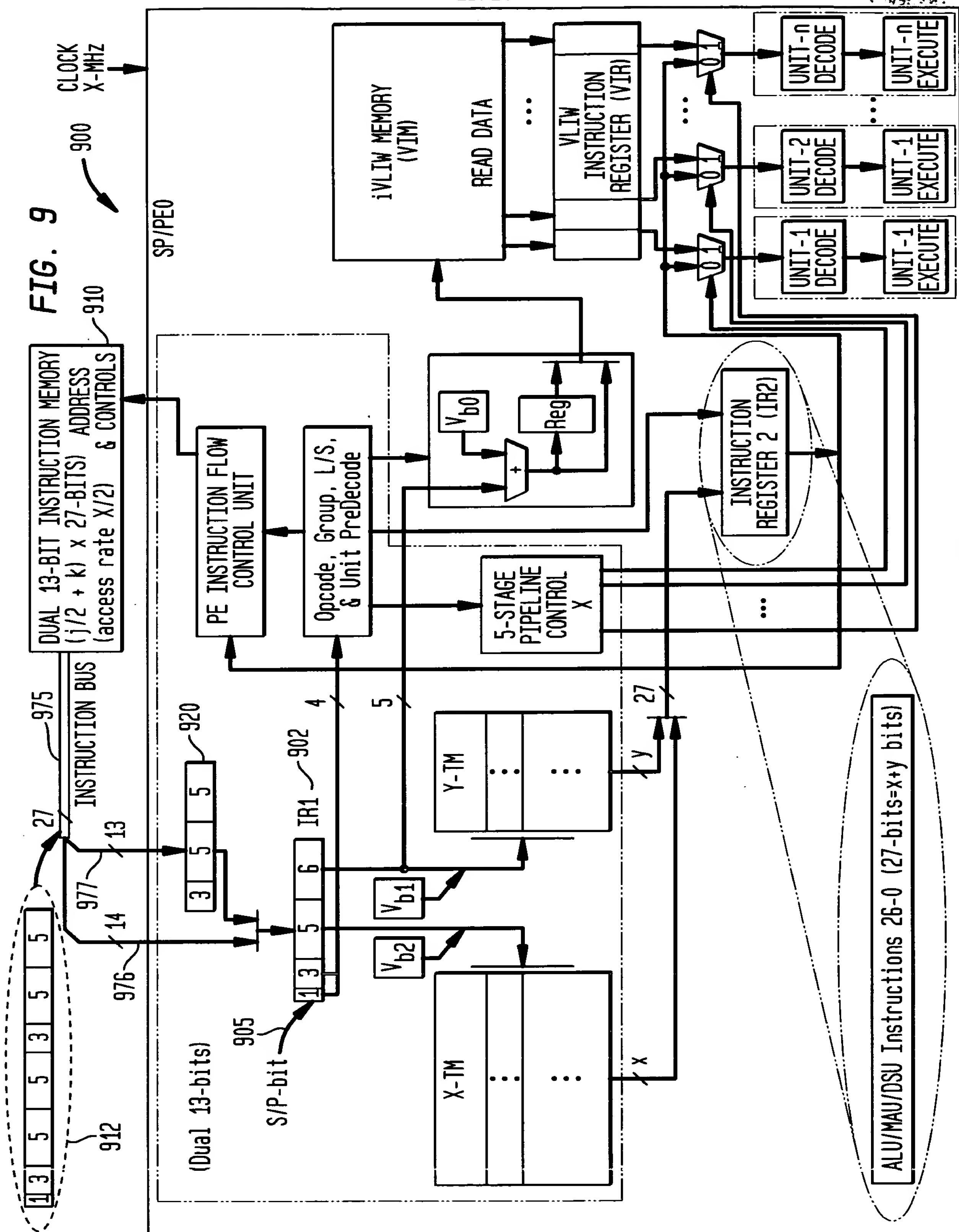
FIG. 8



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FIG. 9



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FIG. 10

CYCLE	FETCH	Xpand & Dispatch	Decode	Execute	Cond. Ret.
1015					
1010~	i SP Fetches a B-bit instruction & loads it into IR1	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)	Previous Instruction Instr(i-4)
1020~	i+1 SP Fetches a B-bit instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i)=ADD.S instruction is loaded into IR2. The S/P-bit and 3-bit opcode are decoded in the S/P.	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)	Previous Instruction Instr(i-3)
1030~	i+2 SP Fetches a B-bit Instr(i+2)=COPY.S instruction & loads it into IR1	S/P-bit opcode indicate an SP XV operation. Local TM fetches occur and a native form of the Instr(i+1)=XV.S instruction is loaded into IR2. The S/P-bit, and 3-bit opcode are decoded in the S/P. The VIM address is calculated and the iVIM is fetched from the XV VIM	The ALU decodes Instr(i)=ADD.S instruction	Previous Instruction Instr(i-1)	Previous Instruction Instr(i-2)
1040~	i+3 SP Fetches a B-bit Instr(i+3)=ADD.S instruction & loads it into IR1	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+2)=COPY.S instruction is loaded into IR2	Instr(i+1)=XV.S causes up to 5 instructions in iVIM decode	The ALU executes Instr(i)=ADD.S instruction	Previous Instruction Instr(i-1)
1050~	i+4 SP Fetches a B-bit instruction: Instr(i+4)	S/P-bit indicates an SP only operation. Local TM fetches occur and a native form of the Instr(i+3)=ADD.S instruction is loaded into IR2	The DSU decodes the Instr(i+2)=COPY.S instruction	Instr(i+1)=XV.S causes up to 5 instructions in iVIM execute	Instr(i+1)=ADD.S side effects are set in ASFs and AGFs